Loss Reduction in Antenna Chip Using Bi-CMOS

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1 INTRODUCTION

State-of-the-art BiCMOS processes have transit frequencies fT well above 200 GHz,making them suitable for new emerging mm-wave applications in the 57-64 GHzband. Several integrated mm-wave antennas on silicon have been published in thepast years with a typical antenna gain below -8 dBi [1]. The low gain is caused bysevere losses in the silicon substrate due to substrate modes propagating through thelow-resistive silicon. The purpose of this work is to present an approach to reducesubstrate losses.

2 SUBSTRATE EFFECT

The cross-section of a typical chip in *CMOS/BiCMOS* technology is illustrated inFig. 1. It is composed of a metal stack, in which an antenna structure can beimplemented, on top of a silicon bulk substrate.The bulk substrate can be considered as aslab waveguide. The cut-off frequencies of theTE-modes of a dielectric slab with infinite lateralextension placed in air can be determinedfrom:-

$$f_c^{(n)} = \frac{n.c_o}{2d_2\sqrt{\varepsilon_{r2} - 1}}, n \epsilon N_o \tag{1}$$

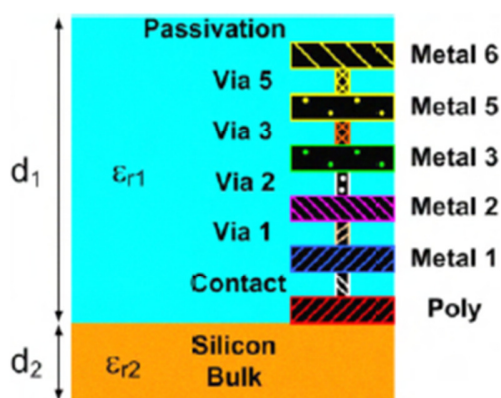*Figure 1:Sketched cross-section of a typical CMOS/Bi-CMOS technology.*

with *n* the mode number, Co the speed of lightin vacuum, *d2* and Er 2 the thickness and permittivityof the slab's material, respectively,[2]. As can be seen from Equation (1) the 0*th*order mode has a 0 Hz cut-off frequency and therefore always gets excited. Since the chip is of finite size the excited substrate modes eventually reach an edge where they get partly reflected and transmitted. The reflection,finally, results in a standing wave between opposite edges. The transmittedpart radiates from the chip's edge and interferes with the waves radiated directlyfrom the antenna and from other edges. This results in a deteriorated antenna radiationpattern which is chip size dependent. Furthermore, the radiation efficiencyis affected by the substrate modes as the high permittivity of the silicon leads to ahigh energy coupling into these modes and the low resistivity of the silicon (usually *p* :S 20 Ωcm) results in high substrate losses. These effects can be well observedfrom the results in Fig. 2. It shows the simulated radiation patterns andefficiencies of a 60 GHz dipole antenna integrated in four chips of 200 /km substratethickness, but different area sizes. The dipoles were placed 50 /km from the chip's edge and the substrate
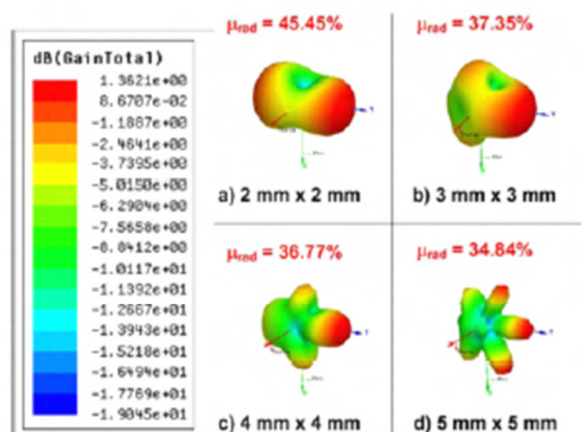

Figure 2: Simulated radiation characteristics of a dipole antenna integrated in chips of different area size.
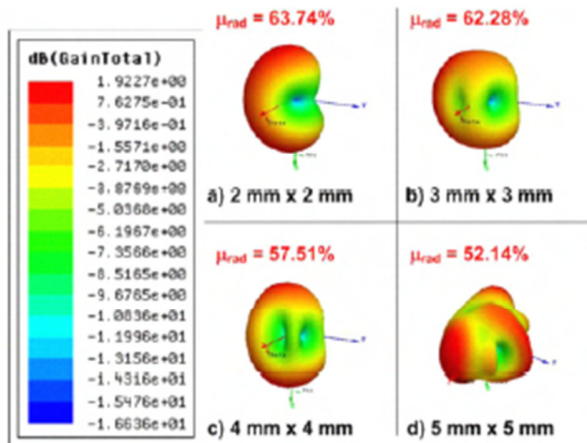
Figure 3: Improved radiation characteristics by coveringthe chip with a metal plate.

resistivity is 20Ω cm. A simple measure that can be takento enhance the off-chip radiation is the implementation of a metal plate coveringthe chip. The substrate can be considered as a surface waveguide for this case withcorresponding surface-wave modes. Assuming the metal plate resides in the Metal1 layer (see Fig. 1), the cut-off frequencies of the TE-modes can be obtained fromthe solutions of the following set of equations ([3]):

$$\tan(\varkappa_{d}) = \frac{d_1}{d_2} C\cot(C\varkappa_{d}) \qquad 2$$

where $\varkappa_{d} = k_0 d_2 \sqrt{\varepsilon_{r2} - 1}$ and $C = \frac{d_1\sqrt{\varepsilon_{r1}-1}}{d_2\sqrt{\varepsilon_{r2}-1}}$

where $k_0 = \omega\sqrt{\varepsilon_0\mu_0}$ is the wave number in free space. The lowest-order TE surfacewavemode is the TE_1 mode. The advantage compared to a slab waveguide is its nonzerocut-off frequency. Hence, for frequencies below cut-off TE-modes are suppressedand the radiation pattern and efficiency is improved. In the semiconductor worldit is already a standard post-processing technique to back-grind the silicon waferto a thickness of 200 /km or lower, while maintaining the mechanical stability forhandling and packaging purposes. With a thickness of 200 */km,* the correspondingcut-off frequency of the TE_1 mode is $_{112}$ GHz, while at 60 GHz the thicknessofthe silicon substrate needs to be well below 350 /km to avoid the TE_1 mode. Onthe right in Fig. 2 the radiation patterns and efficiencies of the on-chip antennas aredepicted when a rectangular metal plate has been added. This plate is placed ata distance of 650 /km from the dipole as shown in Fig. 3 *(r = 650 /km).* Thus, theplate acts as a reflector with the length of the chip's dimension while suppressingthe TE-modes behind the reflecting edge. Hence, the design can be understood asa rudimentary on-chip Vagi-antenna [4]. As can be seen in the figure the radiation pattern does still change with varying chip size, but

the sensitivity of its shapeto the chip's dimension is reduced. The remaining chip size dependence might becaused by the *0th* order TM-mode or the varying reflector length.

3 DESIGN

The metal covered chip approach has been used to design an on-chip antenna. For noise-matching purposes we have chosen Z_{ant}= (30 + j30) Ω as antenna impedance at 60 GHz (direct matching scheme). In the chip design the metal plate is implementedin the lowest metal layer. The transmission line, connecting the dipole
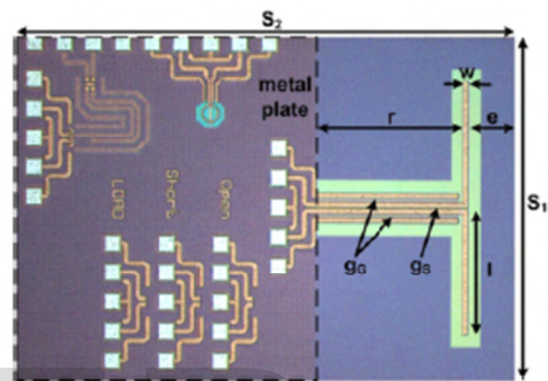
| S_1	S_2	l	w
2 mm	2 mm	540 μm	20 μm
gs	g_G	r	e
6 μm	20 μm	630 μm	50 μm

Figure 4: Chip Design (photograph).

and the RF circuitry above the plate, is similar to those investigated in [5] with acharacteristic impedance Zo = 60 Ω. In the simulation setup the resistivity of thesilicon substrate was set to 200Ωcm which is in agreement with the specificationsof the process used. With the parameters from Fig. 4 the simulated reflection coefficientof the antenna shows a -20 dB bandwidth of 7 GHz around 60 GHz. Theradiation pattern basically looks like the one depicted in Fig. 3 witha maximum directivity of 2.35 dBi and an efficiency of 78.43 %.

4 MEASUREMENT RESULTS AND DISCUSSION

The design from the preceding section has been manufactured in a standard SiGe:CBi-CMOS process. This design differs slightly from the simulation setup, i.e. 81 hasbeen reduced to 1.5 mm and

landing pads have been implemented that are requiredfor the probe-based measurement (see Fig. 3). Additional measurements indicatedthat the silicon bulk resistivity is about 20Ωcm (instead of the specified 200Ωcm)and its thickness is 220 *J-lm*. A comparison of the simulated and measured antennaimpedance is provided in Fig. 5. For this measurement the chips have been gluedon PCB's of 3 mm thickness and a permittivity of 4. The simulation setup has beenadjusted in order to compensate for this. A detailed description of the measurementsetup can be found in [6]. The result still does not entirely match the measured curve.

A reason for the difference might be the simplifications which have been made forthe landing pads model. Furthermore, even-mode reflections introduced by smallasymmetries in the measurement setup could not be measured with our balun. Acomparison of the simulated and measured radiation pattern is also provided inFig. 5. It shows the gain of the on-chip antenna measured from -900 to +900 fromthe normal of the top side of the chip. For the radiation pattern measurementsthe chips were directly glued on a metal plate to avoid the existence of substrate modes in the PCB material. The simulation setup was changed accordingly. Thea symmetry of the E-plane measurement might be caused by reflections from the probe's body which be caused by reflections from the probe's body which might be slightly misaligned to the chip.
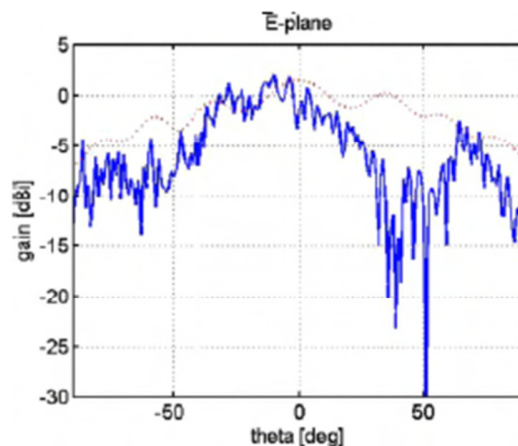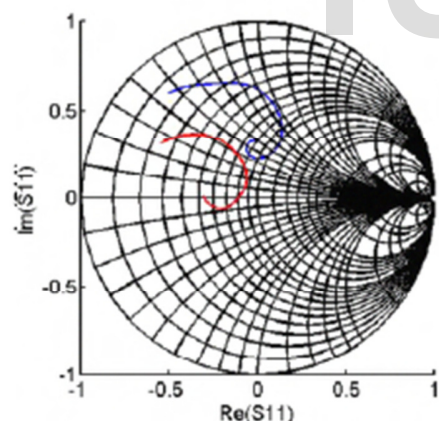
Figure 5: Left: Input reflection coefficient of on-chip antenna for a system impedance of 100 n (red: measurement, blue: simulation). Right: Radiation pattern at 60 GHz(solid: measurement, dashed: simulation).

might be slightly misaligned to the chip. Nevertheless, thecomparison between measured and simulated radiation pattern basically confirms the good radiation efficiency.

5 CONCLUSION

We have explained the effect of the silicon substrate on the off-chip radiation ofan integrated antenna on chip. From this consideration a low-cost approach for an enhanced antenna-on-chip design has been derived and its improved radiation efficiency has been confirmed by measurements.

6 REFERENCES

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